CS-01-049

January 5, 2004

To: Commissioner for Patents
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Subject: Serial No. 10/692,028 10/23/03

Beichao Zhang et al.

VIA ELECTROMIGRATION IMPROVEMENT BY CHANGING THE VIA BOTTOM GEOMETRIC PROFILE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date S.B. Ackerman 1/27/04

U.S. Patent 6,080,660 to Wang et al., "Via Structure and Method of Manufacture," discusses a first etch used to form a via in a dielectric layer above a conductive line and a second etch step used to remove a TiN layer on the metal line as well as part of the metal line.

U.S. Patent 6,004,876 to Kwon et al., "Low Resistance Interconnect for a Semiconductor Device and Method of Fabricating the Same," describes a low resistance interconnect with improved reliability and involves insertion of a Ti reaction prevention layer between a first metal layer and a TiN anti-reflective coating (ARC) on the first metal layer.

U.S. Patent 6,306,732 to Brown, "Method and Apparatus for Simultaneously Improving the Electromigration Reliability and Resistance of Damascene Vias Using a Controlled Diffusivity Barrier," discloses an imperfect diffusion barrier layer at the bottom of a via to control electromigration by reducing stress build up in a metal layer adjacent to a diffusion barrier layer.

U.S. Patent 6,522,013 to Chen et al., "Punch-Through Via with Conformal Barrier Liner," discusses a punch through via with a conformal barrier liner.

U.S. Patent 6,451,181 to Denning et al., "Method of Forming a Semiconductor Device Barrier Layer," describes rounding of via opening corners.

U.S. Patent 6,551,919 to Venkatesan et al., "Method for Forming a Dual Inlaid Copper Interconnect Structure," discloses methods of preventing voids and EM failure.

U.S. Patent 6,383,920 to Wang et al., "Process of Enclosing Via for Improved Reliability in Dual Damascene Interconnects," discusses a barrier layer deposited in a via to reduce voids due to EM.

U.S. Patent 6,069,072 to Konecni et al., "CVD TiN Barrier Layer for Reduced Electromigration of Aluminum Plugs," teaches a CVD TiN barrier to prevent EM failure in an Al plug.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS-01-049	10/692,028
Applicant: Beichao Zhang et al.	
Filing Date: 10/23/03	Group Art Unit

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6080660	6/27/00	Wang et al.	438	637	2/27/98
	6006487	6/21/99	Kwon et al.	438	636	8/14/98
	6306732	10/23/01	Brown	438	468	10/9/98
	6522013	2/18/03	Chen et al.	257	774	8/19/98
	6451181	9/17/02	Denning et al.	204	192.17	3/2/99
	6551919	4/22/03	Venkatesan et al.	438	622	10/3/01
	6383920	5/7/02	Wang et al.	438	639	1/10/01
	6069072	5/30/00	Konecni et al.	438	642	4/15/98

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.